13:40:04 OCA PAD AMENDMENT - PROJECT HEADER INFORMATION 09/29/95

Active

Project #: E-21-Z77 Cost share #: Rev #: 1
Center # : 10/24-6-R8665-0A0 Center shr #: OCA file #:
Work type : RES
Contract#: 5-25563-2 Mod #: P.O.P601809 Document : SUBCONT
Prime #: DAAL01-94-C-0085 Contract entity: GTRC

Subprojects ? : N CFDA: NA
Main project #: PE #: NA

Project unit: ECE Unit code: 02.010.118
Project director(s):
JOKERST N ECE

Sponsor/division names: GEORGE MASON UNIVERSITY / FAIRFAX, VA
Sponsor/division codes: 400 / 111

Award period: 950501 to 960430 (performance) 960430 (reports)

Sponsor amount	New this change	Total to date
Contract value	0.00	20,776.00
Funded	0.00	20,776.00
Cost sharing amount		0.00

Does subcontracting plan apply ?: N

Title: OPTOELECTRONICS INTEGRATED ONTO SILICON VLSI: DEVICES,CIRCUITS SYSTEMS

PROJECT ADMINISTRATION DATA

OCA contact: Ina R. Lashley 894-4820

Sponsor technical contact

DR. RAVINDRA ATHALE
(000)000-0000

GEORGE MASON UNIVERSITY
DEPT. OF ELECTRICAL AND COMPUTER ENG
SCIENCE & TECHNOLOGY BUILDING II
ROOM 229, MAIL STOP 1G5
FAIRFAX, VA 22030

Sponsor issuing office

RITA PICKETTE
(703)993-2984

GEORGE MASON UNIVERSITY
OFFICE OF SPONSORED PROGRAMS
FAIRFAX, VA 22030-4444

Security class (U,C,S,TS) : U ONR resident rep. is ACO (Y/N): N
Defense priority rating : DO-S10 NA supplemental sheet
Equipment title vests with: Sponsor X GIT
NONE PROPOSED OR ANTICIPATED.
Administrative comments -
P.O. #P601809 IS ISSUED FOR BILLING PURPOSES ONLY.

4

GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION

NOTICE OF PROJECT CLOSEOUT

Closeout Notice Date 05/15/96

Project No. E-21-Z77 Center No. 10/24-6-R8665-0A0

Project Director JOKERST N School/Lab ECE

Sponsor GEORGE MASON UNIVERSITY/FAIRFAX, VA

Contract/Grant No. 5-25563-2 Contract Entity GTRC

Prime Contract No. DAAL01-94-C-0085

Title OPTOELECTRONICS INTEGRATED ONTO SILICON VLSI: DEVICES,CIRCUITS SYSTEMS

Effective Completion Date 960430 (Performance) 960430 (Reports)

Closeout Actions Required:	Y/N	Date Submitted
Final Invoice or Copy of Final Invoice	Y	
Final Report of Inventions and/or Subcontracts	Y	
Government Property Inventory & Related Certificate	Y	
Classified Material Certificate	N	
Release and Assignment	Y	
Other	N	

Comments

Subproject Under Main Project No.

Continues Project No.

Distribution Required:

Project Director	Y
Administrative Network Representative	Y
GTRI Accounting/Grants and Contracts	Y
Procurement/Supply Services	Y
Research Property Managment	Y
Research Security Services	N
Reports Coordinator (OCA)	Y
GTRC	Y
Project File	Y
Other	N
	N

NOTE: Final Patent Questionnaire sent to PDPI.

E-21-277
#1

Optoelectronics Integrated Onto Silicon VLSI:

Devices, Circuits, Systems

Final Report

Dr. Nan Marie Jokerst
Associate Professor
School of Electrical and Computer Engineering
Microelectronics Research Center
Manufacturing Research Center
NSF Packaging Research Center
Georgia Tech
Atlanta, GA 30332-0250

April 29, 1996

Contract Prime Number: DAAL01-94-C-0085
Contract Number: 5-25563-2

Optoelectronics Integrated Onto Silicon VLSI: Devices, Circuits, Systems

Final Report

This contract addressed the integration of thin film light emitting diodes onto MOSIS silicon (Si) circuitry. The Si circuitry was designed by attendees of the Georgia Tech short course entitled "Optoelectronics Integrated Onto Silicon VLSI: Devices, Circuits, Systems." This report will outline features of the short course, a description of the thin film LED integration and testing completed for each participant, and a copy of the paperwork that was sent to the participants.

The short course entitled "Optoelectronics Integrated Onto Silicon VLSI Circuits: Devices, Circuits, Systems" was a five full day short course including a hands-on design experience. Features of this course included:

Three days of discussion of hybrid device integration onto Si circuits
- Examination of Si and compound semiconductor detectors and emitters
- Design and operation of analog Si CMOS receivers and transmitters
- Design and operation of digital processing circuitry
- System aspects of integrated optoelectronics
- Design, layout and simulation of analog/digital circuits using MAGIC layout tools

First two evenings:
- Exercises designed to familiarize students with MAGIC layout, extraction, and simulation tools

Third evening, fourth and fifth day:
- Lab for participants to design, layout (using MAGIC), extract, and simulate their own optoelectronic (OE) designs, fully staffed by faculty and graduate student tutors

Students were provided with standard cell designs to use, including:

- Characterized GaAs emitter
- Characterized Si BJT detector
- Analog Si CMOS emitter driver circuit (with external test pads to verify operation)
- Analog Si CMOS detector amplifier circuit
- Digital circuits, including
  - 5 bit digital to analog converter
  - Comparator
  - 1x2, 2x1, 3x1 multiplexers
  - NAND, NOR, XNOR

Tlatch, Dlatch

Note: all standard cell and optoelectronic device performance data were provided in course, i.e., all were fabricated ahead of the course and tested for performance.

Project examples presented included:
- Optical out XNOR
- Optical intensity to frequency
- Multilevel optical IO
- Analog signal processing

Since many students were from companies, proprietary concerns were addressed as follows: students communicated directly with funding agencies regarding operation of their projects, and course instructors were not informed as to operation of each project. However, the instructors and aides carefully examined each project to catch obvious errors, and communicated these errors, when observed, to the course participants to aid in the accuracy of their final submissions.

Testing and delivery:

Due to lengthy MOSIS delays in the p-MOS run (and questions regarding whether a p-MOS run would ever again occur), designs were translated to n-MOS
Designs limited to 1/2 MOSIS TinyChip per project
Designs could access 2 LEDs and any number of detectors per project
Designs were integrated and tested using reserved LED driver/emitter test pads
Fully integrated projects were wire bonded into standard DIP packages for testing

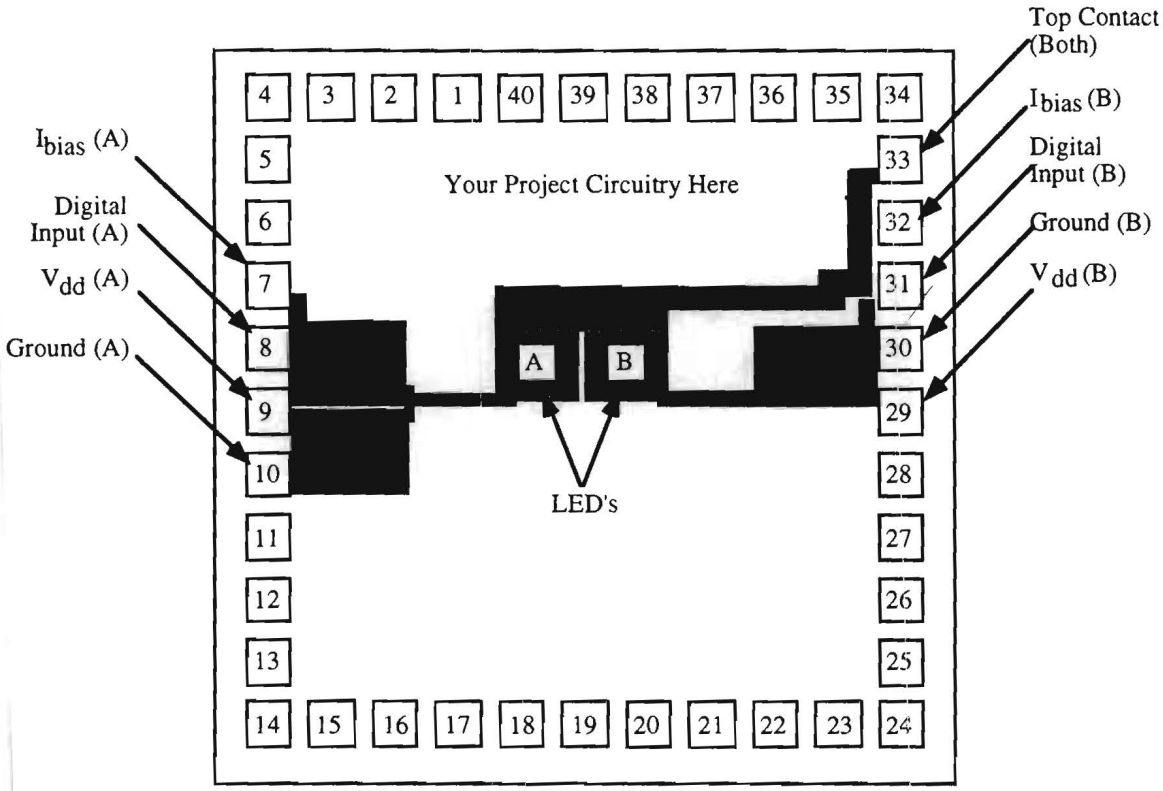
Designs have all been successfully integrated, LEDs verified to emit (see attached photomicrograph of each project delivered to individual participants), and delivered to the participants. Included in the package sent to each participant were instructions for testing, wire bonding diagram the LED driver circuits. Appended are the testing instructions, wire bonding diagram, and a photomicrograph of the (a) fully integrated OEIC circuit (normal lighting conditions, in color) and (b) infrared photomicrograph of the fully integrated OEIC circuit with the two emitters per project emitting. Note that the normal light conditions circuits are showing only 1/2 chip (a single project) for proprietary purposes.

Bottom

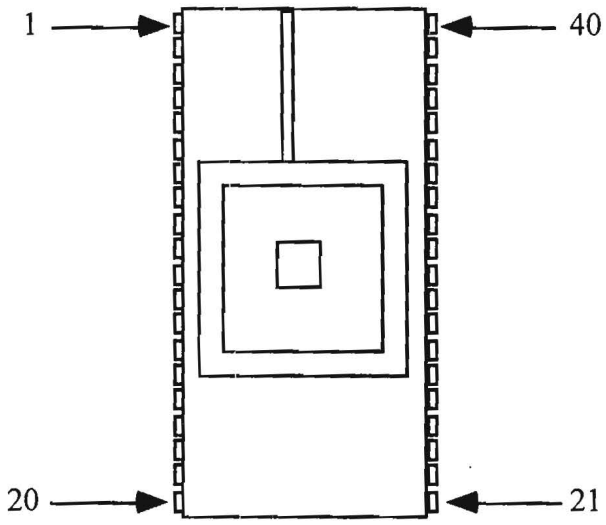
Instructions for Testing the LED Driver Circuits

The LED driver circuit has both power supply (PS) connections (V_{dd} at pins 9 & 29, GND at pins 10 & 30; these are independent from the project circuitry) and two controlling inputs (digital control (0 V enable, 5 V disable) at pins 8 & 31; and analog control (I_{bias}) at pins 7 & 32). The circuit is designed to operate with 5 Volts between V_{dd} and GND. The top contact of the LED has it's own lead (pin 33), so that it can be biased independently of the circuits, and nominally operates best between -1 and +3 Volts. The PS and control pins associated with the LED on the right (nearest pin 40): 32 (I_{bias}), 31 (Digital input), 29 (V_{dd}), 30 (GND), & 33 (LED top contact). For the LED on the left corner (nearest pin 1): 7 (I_{bias}), 8 (Digital input), 9 (V_{dd}), 10 (GND), & 33 (LED top contact).

To find the best operating parameters for your LED and driver, start with 5 Volts between V_{dd} and GND, and the LED top contact at 0 Volts (this is best accomplished with a separate power supply between this pin and ground, rather than just tying it to GND, because you may find that the LED requires more (-1 Volt at this pin, for example) or less biasing voltage (+3.5 Volts at this pin, for example)). Initially , the digital input can just be tied low (ground level), which signals the LED to be turned on. If you have access to a current source, pulling up to 100 µA from the analog input (I_{bias}) will then turn the LED on (increasing this current increases the brightness of the LED; 100 µA should be considered the limit though); without a current source, this can be accomplished with a potentiometer: tie the potentiometer's fixed leads between V_{dd} and GND and the wiper to the analog input; start with the wiper at V_{dd} and the LED will brighten as it is turned toward GND (the voltage at the wiper should be somewhere between +3.5 and +2.0 Volts when the LED first turns on). Remember that this is an IR LED, and as such it's emission can not be seen with the naked eye; current through the top contact may be used as an indication that the LED is on. If the LED does not turn on when 100 µA are pulled from the analog input pin (or the potentiometer reaches GND at the wiper), leave this signal at maximum and increase the top contact bias voltage (increasing the bias voltage in this case means making the voltage at this pin more negative; don't exceed -5 volts though). If the LED pulls too much current (i.e., it pulls over 25 mA through the top contact pin or appears excessively bright), decrease the top contact bias voltage (which in this case means to make the voltage at this pin more positive). To verify that the driver's digital control functions, switch the digital control pin high (to V_{dd}) and the LED will extinguish.



Circuit Layout Showing Package Pin Numbers



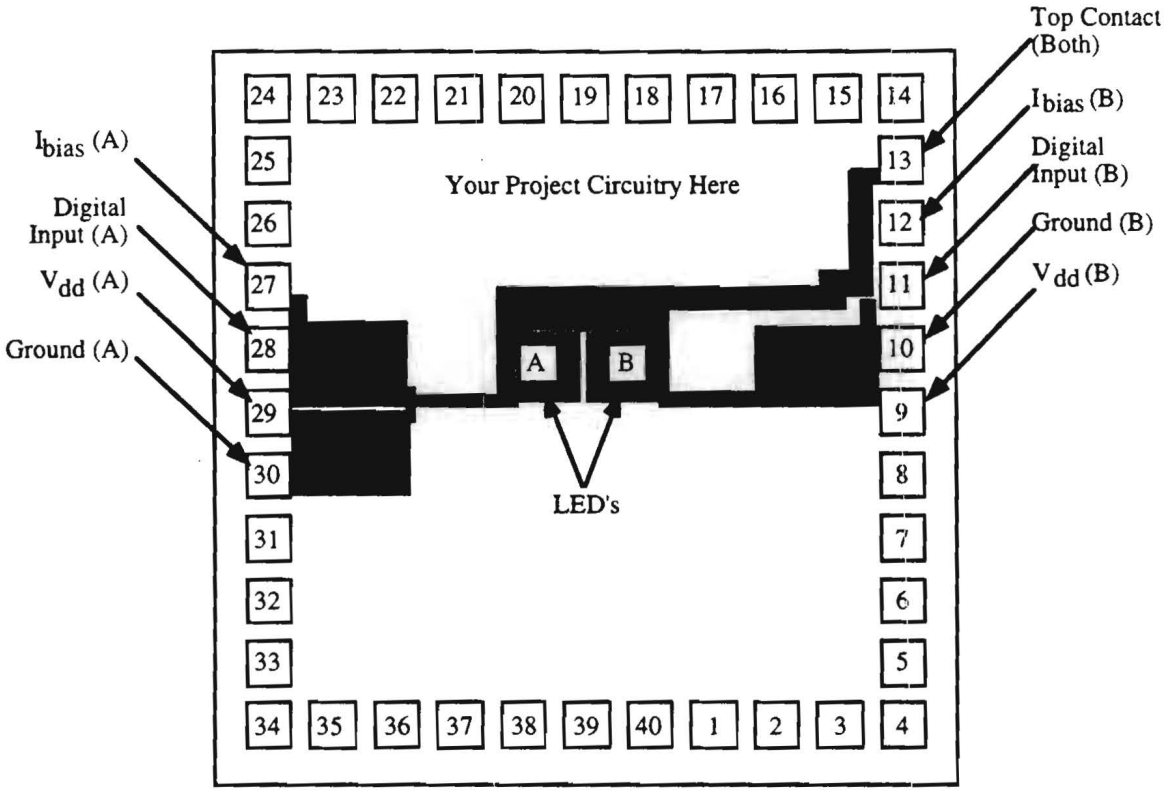
Package Layout Showing Pin Numbers

Top

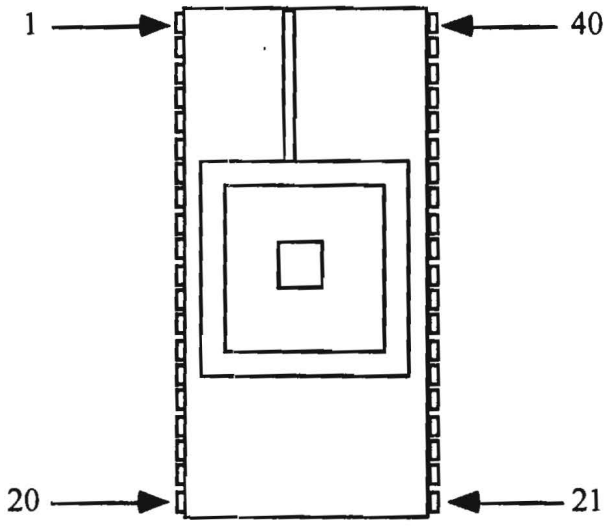
Instructions for Testing the LED Driver Circuits

The LED driver circuit has both power supply (PS) connections (V_{dd} at pins 9 & 29, GND at pins 10 & 30; these are independent from the project circuitry) and two controlling inputs (digital control (0 V enable, 5 V disable) at pins 11 & 28; and analog control (I_{bias}) at pins 12 & 27). The circuit is designed to operate with 5 Volts between V_{dd} and GND. The top contact of the LED has it's own lead (pin 13), so that it can be biased independently of the circuits, and nominally operates best between -1 and +3 Volts. The PS and control pins associated with the LED on the left (nearest package pin 21) are: 27 (I_{bias}), 28 (Digital input), 29 (V_{dd}), 30 (GND), & 13 (LED top contact). For the LED on the right (nearest pin 20): 12 (I_{bias}), 11 (Digital input), 9 (V_{dd}), 10 (GND), & 13 (LED top contact).

To find the best operating parameters for your LED and driver, start with 5 Volts between V_{dd} and GND, and the LED top contact at 0 Volts (this is best accomplished with a separate power supply between this pin and ground, rather than just tying it to GND, because you may find that the LED requires more (-1 Volt at this pin, for example) or less biasing voltage (+3.5 Volts at this pin, for example)). Initially , the digital input can just be tied low (ground level), which signals the LED to be turned on. If you have access to a current source, pulling up to 100 μA from the analog input (I_{bias}) will then turn the LED on (increasing this current increases the brightness of the LED; 100 μA should be considered the limit though); without a current source, this can be accomplished with a potentiometer: tie the potentiometer's fixed leads between V_{dd} and GND and the wiper to the analog input; start with the wiper at V_{dd} and the LED will brighten as it is turned toward GND (the voltage at the wiper should be somewhere between +3.5 and +2.0 Volts when the LED first turns on). Remember that this is an IR LED, and as such it's emission can not be seen with the naked eye; current through the top contact may be used as an indication that the LED is on. If the LED does not turn on when 100 μA are pulled from the analog input pin (or the potentiometer reaches GND at the wiper), leave this signal at maximum and increase the top contact bias voltage (increasing the bias voltage in this case means making the voltage at this pin more negative; don't exceed -5 volts though). If the LED pulls too much current (i.e., it pulls over 25 mA through the top contact pin or appears excessively bright), decrease the top contact bias voltage (which in this case means to make the voltage at this pin more positive). To verify that the driver's digital control functions, switch the digital control pin high (to V_{dd}) and the LED will extinguish.

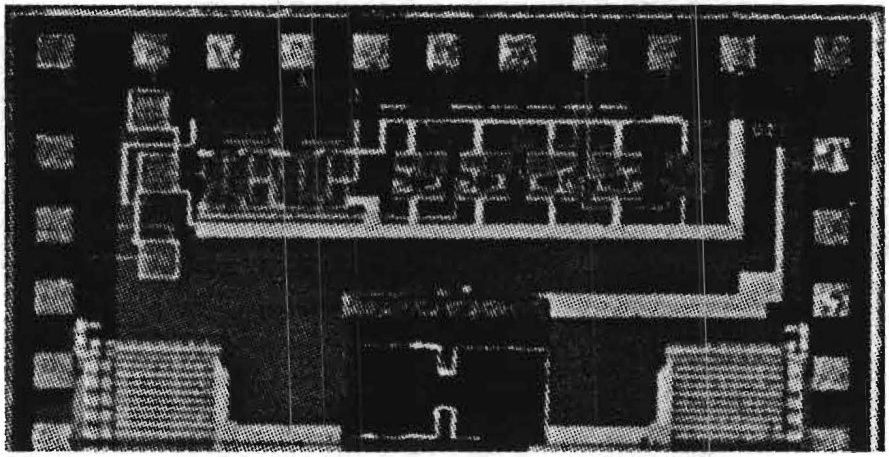


Circuit Layout Showing Package Pin Numbers

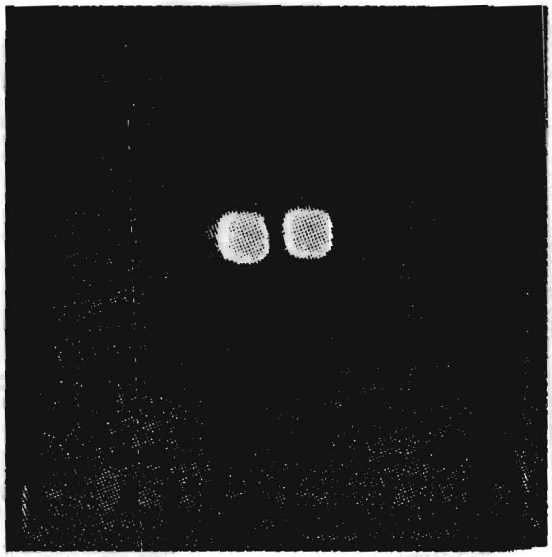


Package Layout Showing Pin Numbers

CWBottom

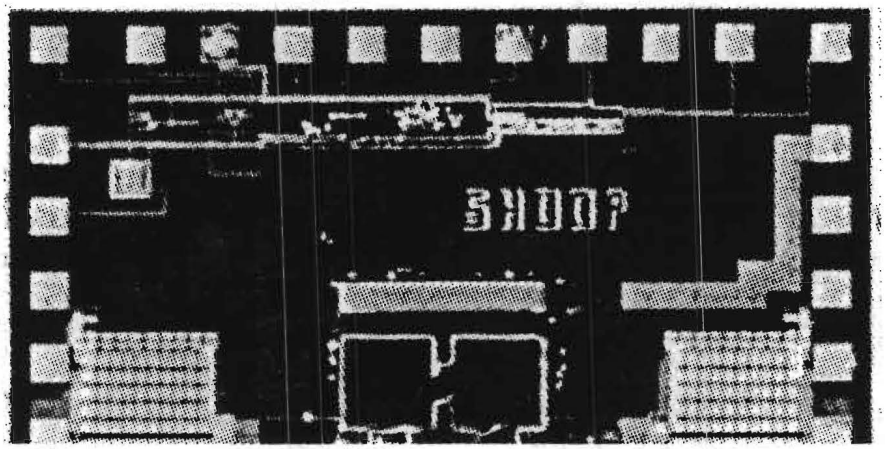


Completed Project with Two Integrated LED's.



Infrared Photomicrograph of Project with Both LED's Under Test.

DFBottom



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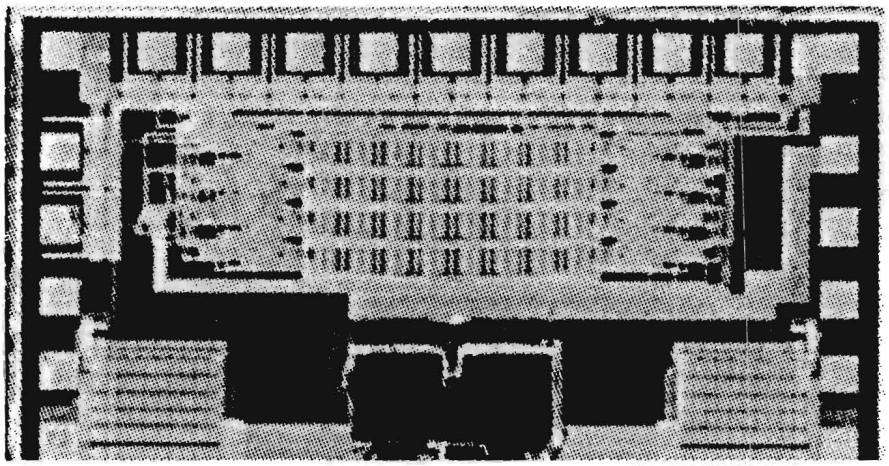

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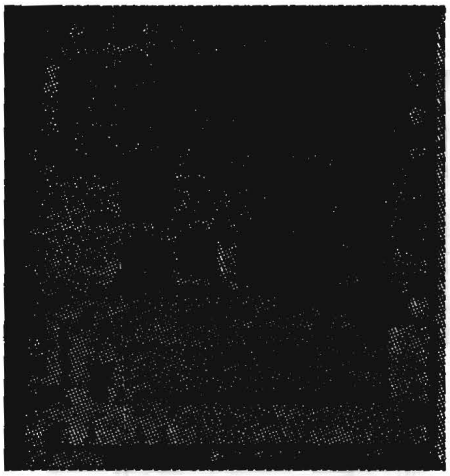
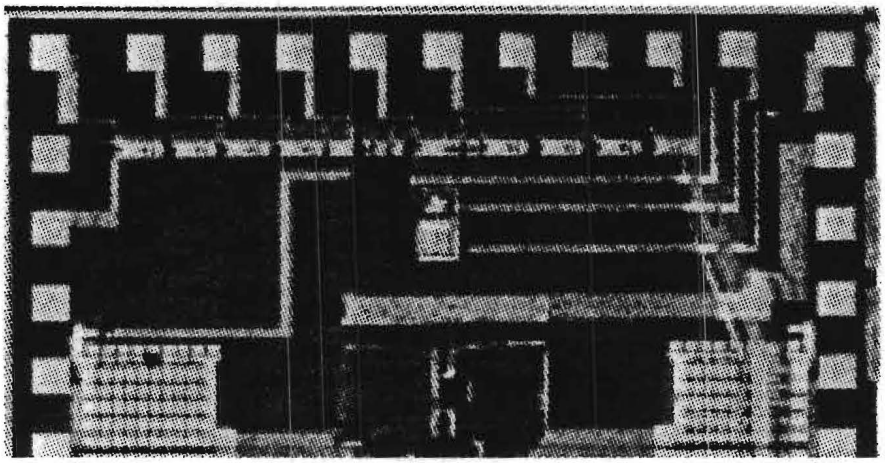


Infrared Photomicrograph of Project with Both LED's Under Test.

DTBottom



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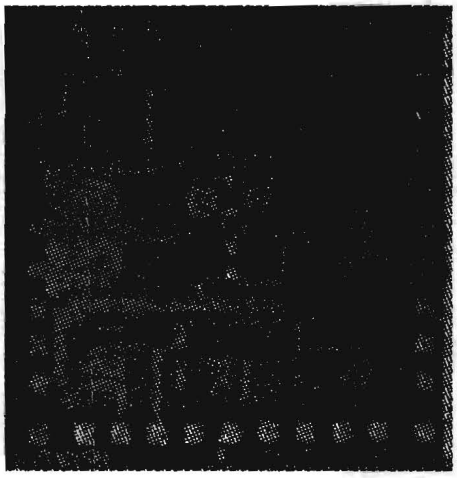
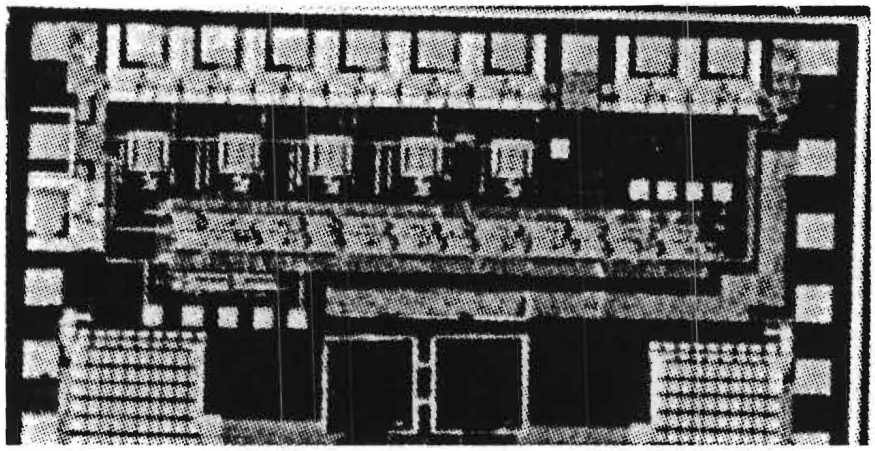
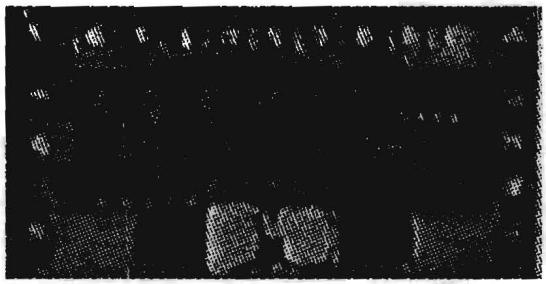


Infrared Photomicrograph of Project with Both LED's Under Test.

D Bottom



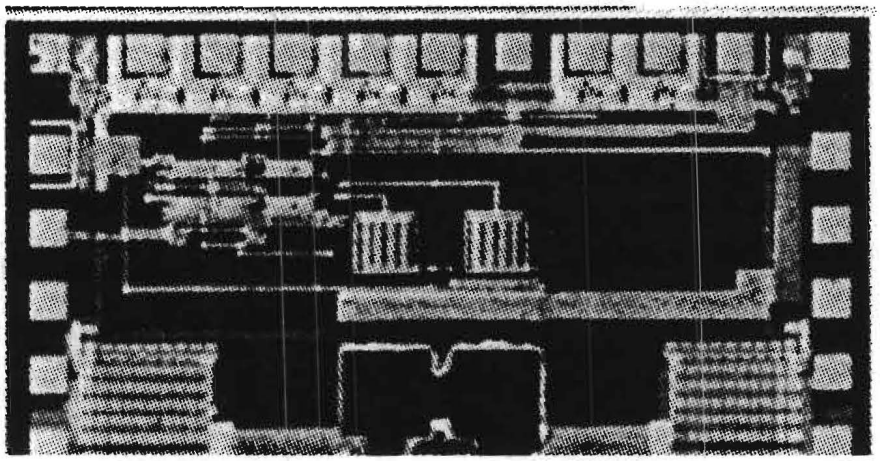
Completed Project with Two Integrated LED's.



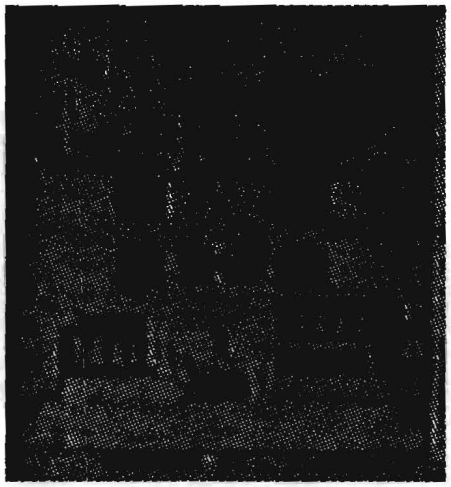
Infrared Photomicrograph of Project with Both LED's Under Test.

DWBottom

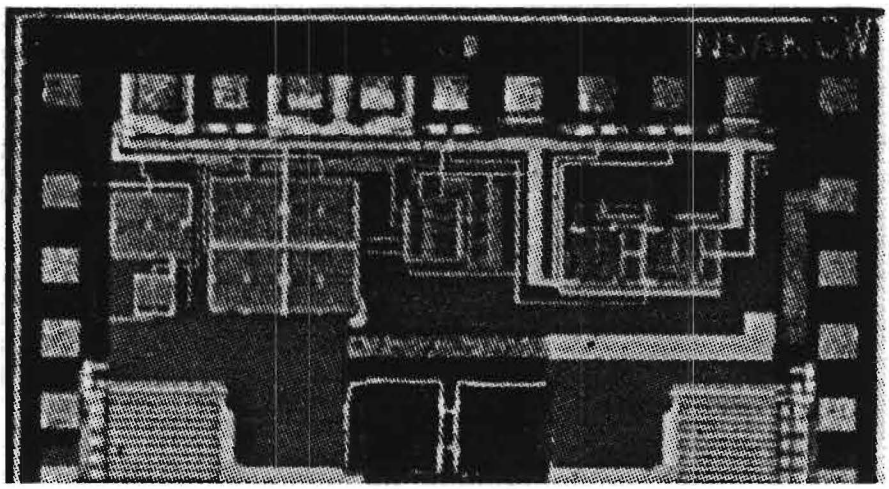
Insert Descripion/Testing here.



Completed Project with Two Integrated LED's.



Infrared Photomicrograph of Project with Both LED's Under Test.



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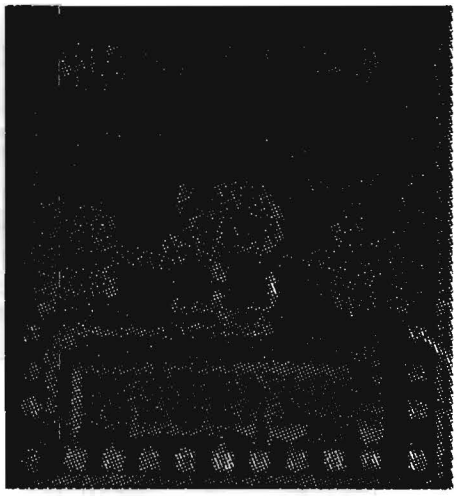
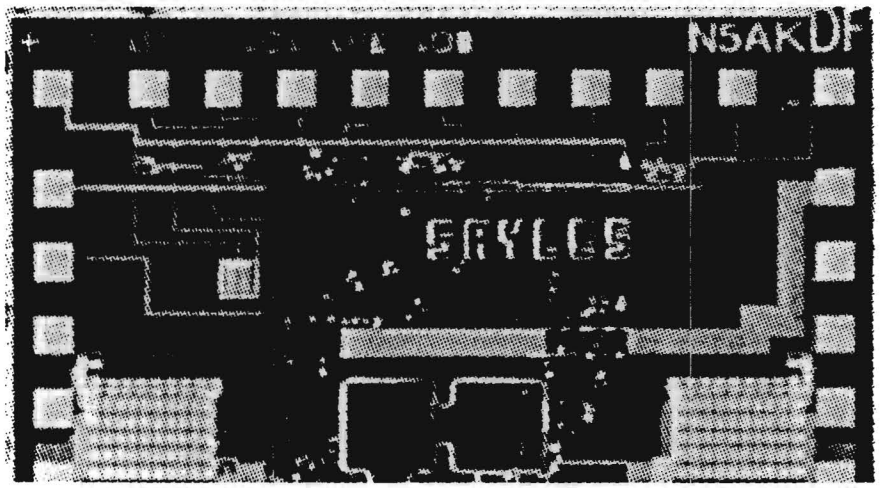


Infrared Photomicrograph of Project with Both LED's Under Test.

DFTop



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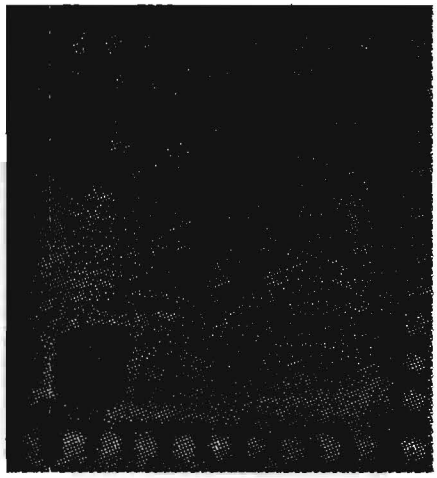

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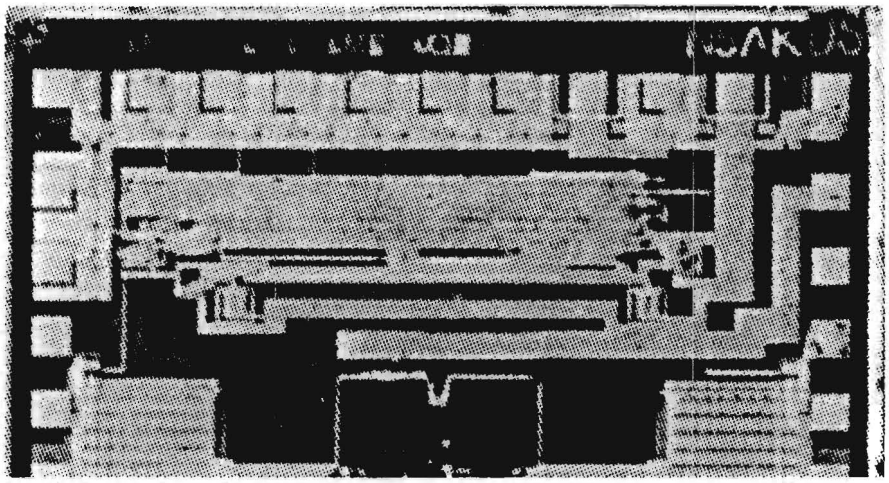

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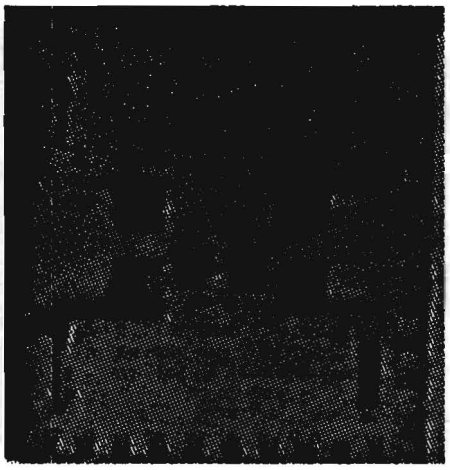

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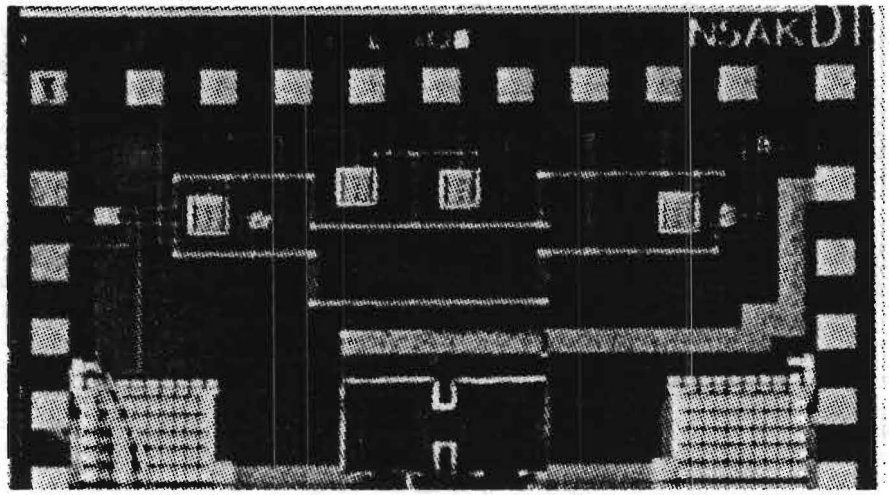
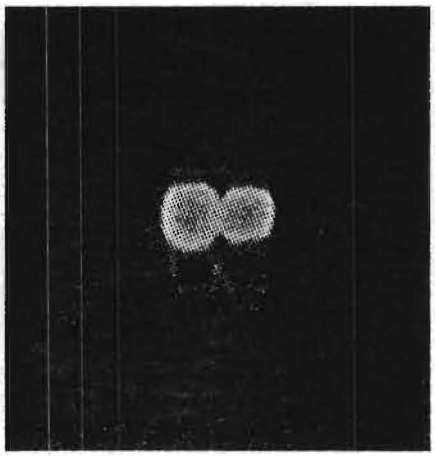
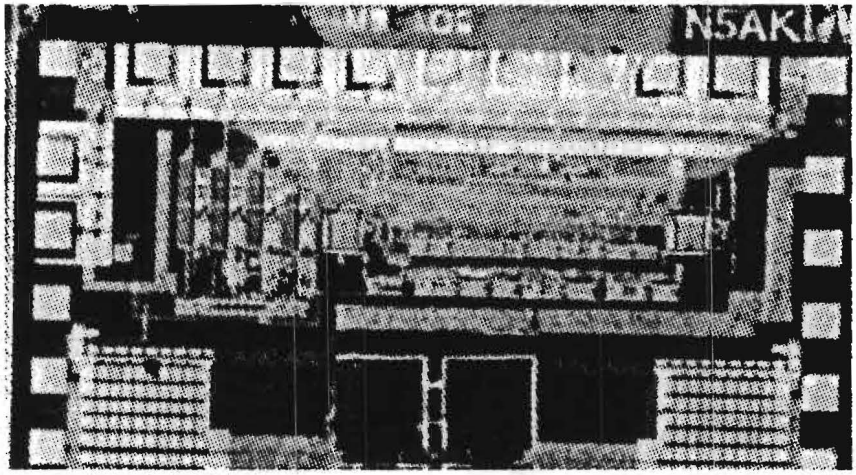


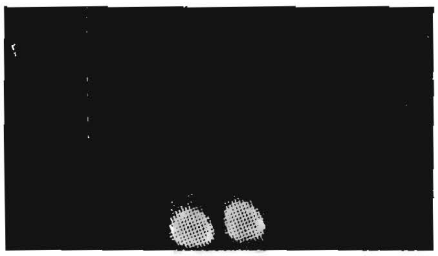
Completed Project with Two Integrated LED's.



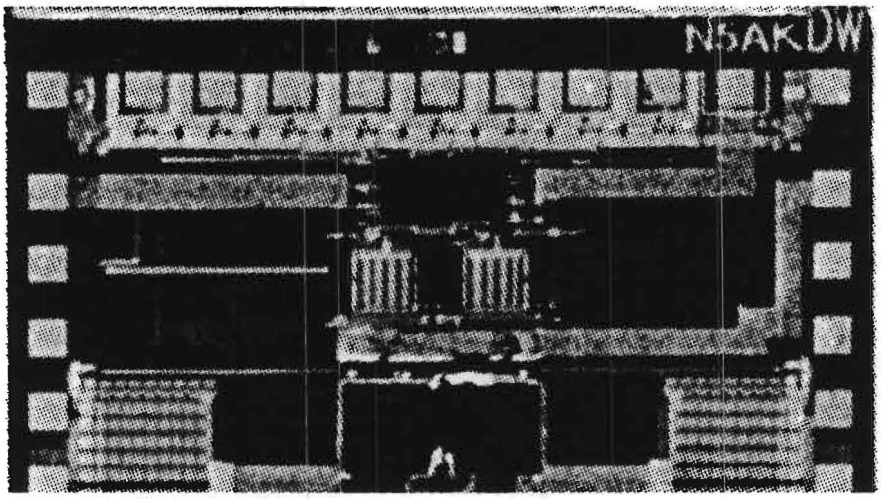
Infrared Photomicrograph of Project with Both LED's Under Test.



Completed Project with Two Integrated LED's.



Infrared Photomicrograph of Project with Both LED's Under Test.



Completed Project with Two Integrated LED's.

Infrared Photomicrograph of Project with Both LED's Under Test.